

AN-810 Semiconductor Products Inc. P.O. BOX 2014 CONDUCTOR DE Application Note

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# **DUAL 16-BIT PORTS FOR THE MC68000** USING TWO MC6821S

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The MC6821 Peripheral Interface Adapter (PIA) is a 40-pin device having two 8-bit ports. Each port has its own control register and may be configured as input or output on a bit-by-bit basis.

MOTOROLA

Two PIAs may be configured on the MC68000 microprocessor bus to give two 16-bit ports. The ability of the MC68000 to simultaneously access 16 bits of data at an effective rate of up to two megahertz makes it ideal for processing applications using state-of-the-art A/D or D/A converters. The MC68000 is also suited for applications involving advanced peripherals with parallel inputs or outputs and a high data throughput rate.

# **ASYNCHRONOUS OPERATION**

The schematic for the MC68000/MC6821 asynchronous interface appears in Figure 1. Typical timing diagrams appear in Figure 2. Edge connector designations for MC68000 signals correspond to the MEX68KDM Design Module bus pin allocations (EXORciser bus). The asynchronous interface is responsible for three major tasks:

- Detecting when the PIAs are being addressed
- Synchronizing the MC68000 bus cycle to the local E clock
- Controlling data flow to and from the PIAs

Bus Buffering - Buffers U1, U2, U3, U16, U17, U18, and U19 are all microprocessor bus buffers/drivers which make this design compatible with the MEX68KDM Design Module. Other buffering schemes may be more appropriate in other applications. In particular, buffers U5, U6, U7 and U8 will provide sufficient data bus buffering in a system where the data bus is not inverted.

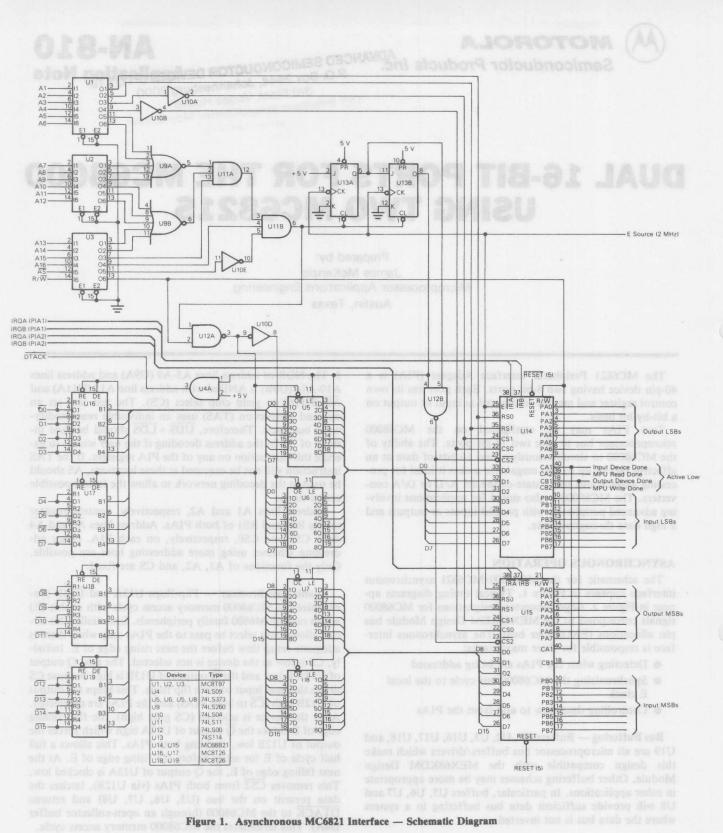
Address Decoding - The two PIAs are located at \$18000-\$18007, as shown in the memory map given in Figure

3. The NOR of address lines A5-A9 (U9A) and address lines A10-A14 (U9B) is ANDed with address line A15 (U11A) and AS (U11B) to yield chip select (CS). The test and set an operand instruction (TAS) uses an indivisible read-modifywrite bus cycle. Therefore, UDS + LDS should be used instead of AS in the address decoding if the user wishes to execute this instruction on any of the PIA registers. If the TAS instruction will not be executed at these locations, AS should be used in the decoding network to allow the fastest possible access times.

Address lines A1 and A2, respectively, control register selects RS0 and RS1 of both PIAs. Address lines A3 and A4 drive CS1 and CS0, respectively, on each PIA. Other addressing schemes using more addressing lines are possible. Only the functions of A1, A2, and CS are fixed.

Enable Synchronizer - Flip-flops U13A and U13B synchronize the MC68000 memory access cycle with enable (E) which runs all M6800 family peripherals. Essentially, this circuit allows chip select to pass to the PIAs only when there is adequate setup time before the next rising edge of E. Initially, CS is low as the device is not selected. The next Q output of U13A is low and the Q output of U13B is high because CS drives the clear input of both flip flops. This keeps the output of U12B high (CS to both PIAs) and the PIAs are deselected. After the device is selected (CS goes high), the first falling edge of E clocks the  $\overline{Q}$  output of U13A high which forces the output of U12B low, enabling both PIAs. This allows a full half cycle of E for setup before the rising edge of E. At the next falling edge of E, the Q output of U13A is clocked low. This removes CS2 from both PIAs (via U12B), latches the data present on the bus (U5, U6, U7, U8) and returns DTACK to the MC68000 through an open-collector buffer U4A). This terminates the MC68000 memory access cycle.

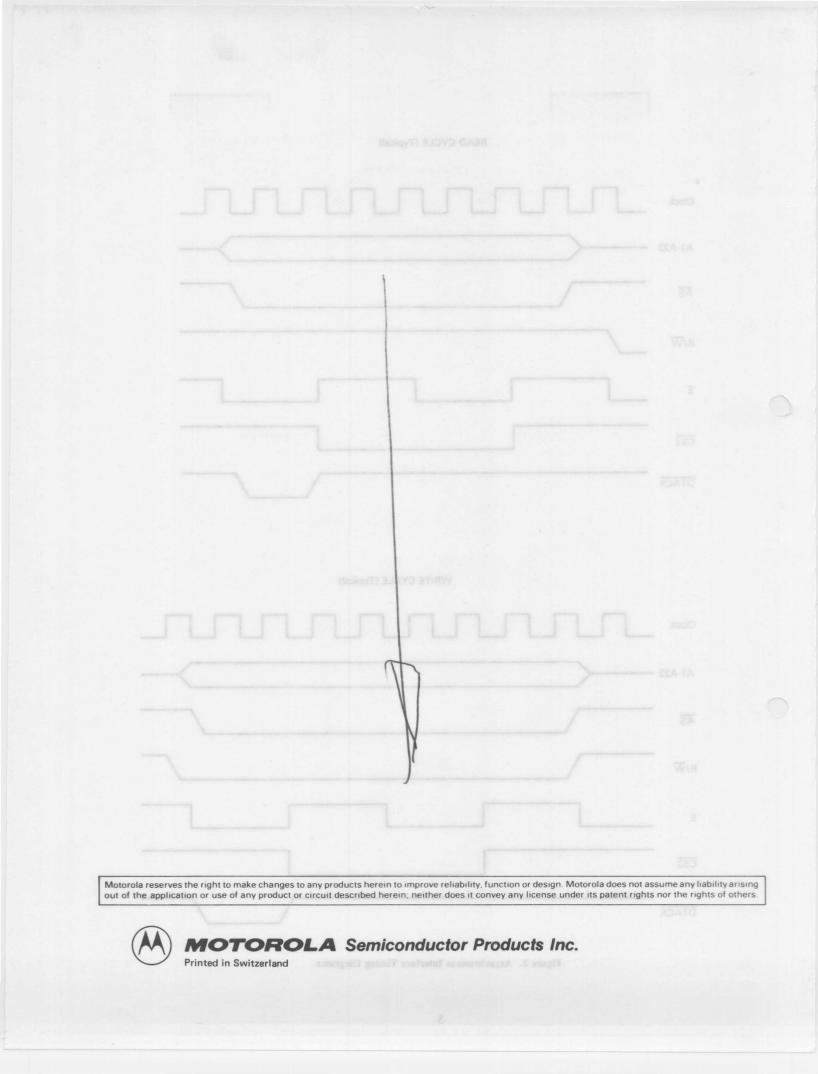
If a fifty percent duty cycle, two megahertz E signal is used a best case access cycle time of 875 nanoseconds and a worst case access cycle time of 1375 nanoseconds will be obtained.



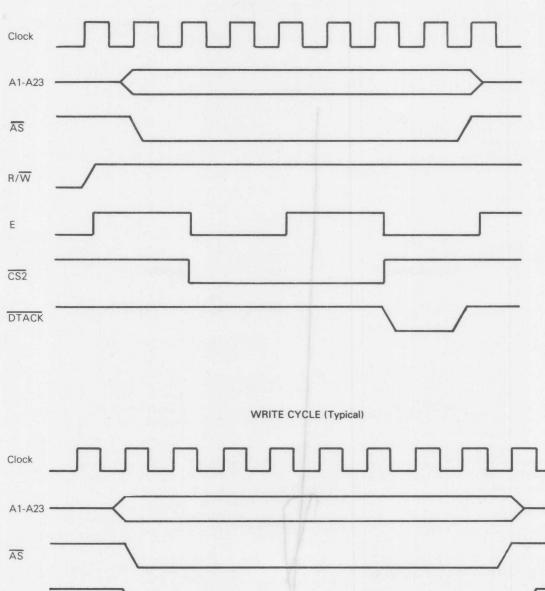
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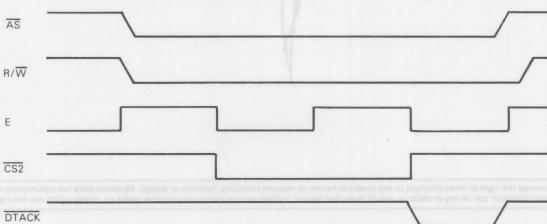
Address Decoding --- The two PIAs are located at \$18000-\$18007, as shown in the memory map given in Figure

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READ CYCLE (Typical)







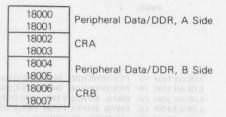


Figure 3. Memory Map

**Bus Buffers Enables** — Gates U12A and U10D coordinate the flow of data on the bidirectional data bus to and from the PIAs. These gates form the Boolean equation  $\overline{R/W} \circ CS$  (pin 3, U12A) which gates the flow of data to and from the PIAs on U16, U17, U18, and U19. Data is allowed to flow from the PIAs to the MC68000 bus through latches U5 and U7. Also, the signal  $R/\overline{W} \circ CS$  (pin 8, U10D) allows data to pass from the MC68000 bus to the PIAs through latches U6 and U8. Latches U5, U6, U7, and U8 guarantee that valid data is on the bus throughout the MC68000 cycle, not just when the PIAs are selected.

## SYNCHRONOUS OPERATION

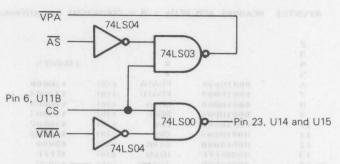
The MC68000 can control M6800 synchronous parts directly using the M6800 peripheral control bus. This bus consists of enable (E), valid memory address ( $\overline{VMA}$ ), and valid peripheral address ( $\overline{VPA}$ ). The two 16-bit ports may be operated synchronously by replacing U13, U12B, and U4A of Figure 1 with the circuitry shown in Figure 4. Valid peripheral address ( $\overline{VPA}$ ), a wire-ORed signal, is returned by an open-collector NAND gate when the chip select is detected. As the processor responds with  $\overline{VMA}$ , the PIAs are selected (pin 6, U12B). Enable (E) is provided by the MC68000 in this case and has the frequency of the system clock divided by eight. The MC68000 must synchronize  $\overline{VMA}$  with E internally, so this method does not allow as fast an access as the asynchronous interface.

### SOFTWARE CONSIDERATIONS

Because the upper and lower data strobes (UDS, LDS) are not used in address decoding, an individual PIA cannot be accessed. However, word operations on the MC68000 must begin access on an even address. Therefore, the user must take care to address the registers of the PIA with an even address. If individual access is desired, address line A3 could be shifted into the address decoding network and LDS applied to CS1 of U14 through an inverter. Likewise, UDS could then be applied to CS1 of U15 through an inverter. This would result in the memory map shown in Figure 5.

### **PERIPHERAL CONTROL LINES**

The configuration and labeling of the peripheral control lines (CA1, CA2, CB1, CB2) for the PIAs in Figure 1 is for a 16-bit input port (A sides of each PIA) and a 16-bit output port (B sides) each programmed for handshake operation. Any of the other configurations of these control lines is possible. The most desirable configuration will depend on the type of peripheral equipment being interfaced and its application. A typical initialization routine for the configuration shown in Figure 1 is given in Figure 6.



Note: When VMA is used, AS should be disconnected from the CS decoding (Figure 1, U11B) and that input is tied active.

Figure 4. Synchronous Interface Circuitry

| 18000 | Peripheral Data/DDRA | (U15) |
|-------|----------------------|-------|
| 18001 | Peripheral Data/DDRA | (U14) |
| 18002 | CRA                  | (U15) |
| 18003 | CRA                  | (U14) |
| 18004 | Peripheral Data/DDRB | (U15) |
| 18005 | Peripheral Data/DDRB | (U14) |
| 18006 | CRB                  | (U15) |
| 18007 | CRB                  | (U14) |

Figure 5. Alternative Memory Map

# **MODES OF OPERATION**

The PIAs may be operated in one of two basic modes, polled or interrupt driven. Polling can cause excessive execution time overhead when more than just a few peripherals are on the bus, so interrupts are usually an attractive alternative. There are many ways to run an interrupt driven system, especially on the MC68000 which has seven priority levels of interrupt and can handle up to 192 unique user interrupt vectors. The MC68000/MC6821 interface yields four interrupt request lines giving a high degree of versatility for interrupting, regardless of the prioritizing scheme used or whether the PIAs are configured as 8-bit ports, 16-bit ports or a combination of both.

### **32-BIT PORTS**

If address line A1 is allowed to drive RS1 and address line A2 drives RS0, then the peripheral data registers for the two PIAs will occupy four consecutive locations of memory beginning at \$18000. This location may be used as a 32-bit input or output port. Control register A would be located at \$18004 and control register B would be at \$18006. Keep in mind that these last two registers are each 16 bits wide, as shown in Figure 7. The 32-bit port could be accessed with long word attribute op codes such as:

MOVE.L \$18000,D0

# CONCLUSION

Two PIAs provide an excellent parallel I/O port for the MC68000 and are easily interfaced to the standard asynchronous bus. If B series parts are used, the PIAs may be accessed at effective rates of greater than 1.0 megahertz.

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| <ul> <li></li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| <ul> <li></li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 3      |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| 1       00015800       PDATA<br>F004TES       F004TES         2       00016800       PDATA<br>F001 F801       F004 f8000       L0CatIon 0F PERTPERAd Data REGISTER 8<br>L0CatIon 0F PERTPERAd Data REGISTER 8<br>L0CatIon 0F PARTA DERCIDER F80         3       00018802       CRA       F001 f8003       L0CatIon 0F PERTPERAd Data REGISTER 8<br>L0CatIon 0F Common Register 8<br>L0CatIon 0F Comm                        |        |            |                   | *            |                 |                      |         |        |                |                |              |                |           |
| 5       00016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0016000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000       0006000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |            |                   |              | F               | QUATES               |         |        |                |                |              |                |           |
| 4       00016000       PDATA       FUU       + 16000       LOCATING 0F FERTMERAL DATA RECUSTER A         7       00016001       PDATA       FUU       + 16000       LOCATING 0F FERTMERAL DATA RECUSTER A         9       00016001       DDRA       FOU       + 16000       LOCATING 0F FERTMERAL DATA RECUSTER A         9       00016001       DDRA       FOU       + 16000       LOCATING 0F FERTMERAL DATA RECUSTER A         10       00016002       CNA       FOU       + 16002       LOCATING 0F FERTMERAL DATA RECUSTER A         11       00016002       CNA       FOU       + 16002       LOCATING 0F FERTMERAL DATA RECUSTER A         12       0001000       DTRA       FOU       + 16002       LOCATING 0F CONTRUE RECUSTER A         13       0001602525       TNTTA       FOU       + 16006       SETS ALL 16 A TINES AS IMPUTS         14       0001000       ACMAR       FOU       + 2525       WALE TO ACCESS DORA       THROUCH CRA         15       0010000       ACMAR       FOU       + 2525       WALE TO ACCESS DORA       THROUCH CRA         16       0001000       ACMAR       FOU       + 40000       WALE TO ACCESS DORA       THROUCH CRA         17       0000000       ACMAR       + 4000RA                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| 9       00018000       DDBse       FeI       \$18001       LCCATTCM OF DATA DIRECTION RECISTER A         10       00018002       CKA       EGU       \$18002       LCCATTCM OF DATA DIRECTION RECISTER A         11       00018002       CKA       EGU       \$18003       LCCATTCM OF DATA DIRECTION RECISTER A         12       0001000       CHA       FOU       \$18004       LCCATTCM OF CONTROL RECISTER A         13       00007525       INTIA       FOU       \$18006       SETS ALL 16 A LINES AS UPUTS         14       00002525       INTIA       FOU       \$2575       WALUE TO INTIALIZE CRA         14       00002525       INTIA       FOU       \$2575       WALUE TO ACCESS DORS THROUGH CRA         15       0000000       ACDRA       FOU       \$1000       WALUE TO ACCESS DORS THROUGH CRA         16       0000000       ACDRA       FOU       \$1000       WALUE TO ACCESS DORS THROUGH CRA         16       0000000       ACDRA       FOU       \$1000       \$2575       WALUE TO ACCESS DORS THROUGH CRA         17       0000000       ACDRA       FOU       \$10000       ACCESS DORS THROUGH CRA       \$1001000         20       00018002       MOVE.4       \$10070.4       \$1000000       \$100                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 6      |            | 00018600          | PDATA        | EQU             | +18000               |         |        | LOCATION       | OF PERTPI      | ERAL.        | DATA RE        | EGISTER A |
| 9       00018002       CAA       600       418004       CCCATICS OF CONTROL RECISTER E         10       00018002       CKA       600       418002       CCCATICS OF CONTROL RECISTER A         12       00000000       CKA       600       418004       CCCATICS OF CONTROL RECISTER A         13       00000-FFF       DIRE       E00       418004       CCCATICS OF CONTROL RECISTER A         14       00002525       INTTE       E00       41575       Walle TO       10111114 IZE CKA         16       00000000       ACDEA       E00       40000       Walle TO       IAITTALIZE CKA         18       C00000000       ACDEA       E00       40000       Walle TO       IAITTALIZE CKA         10       00018002       FOU       410000       Walle TO       IAITTALIZE CKA         10       00018002       <                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 7      |            | 00018004          | PDATE        | EDU             | \$18004              |         |        | LOCATION       | OF FERIFI      | HERAL        | DATA RE        | EGISTER B |
| 10       00018002       CKA       End       \$18002       COATION OF CONTROL REGISTER A         11       00010000       OTEA       F00       \$10000       SETS ALL 16 A 1 INES AS UNFUTS         13       0000000       SETS ALL 16 A 1 INES AS UNFUTS       SETS ALL 16 A 1 INES AS UNFUTS         14       0000000       ACD6A       F00       \$16000       SETS ALL 16 A 1 INES AS UNFUTS         14       0000000       ACD6A       F00       \$2555       W41UE TO INTIALIZE CEA         15       0000000       ACD6A       F00       \$10000       W41UE TO ACCESS DDFA THROUGH CRA         16       0000000       ACD6A       F00       \$10000       W41UE TO ACCESS DDFA THROUGH CRA         16       0000000       ACD6A       F00       \$10000       W41UE TO ACCESS DDFA THROUGH CRA         17       0000000       ACD6A       F00       \$10000       W41UE TO ACCESS DDFA THROUGH CRA         18       00018000       F00       F00       F00       F00       F00         20       00018000       F00       F00       F00       F00       F00         20       00018000       F00       F00       F00       F00       F00       F00         20       00018000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 8      |            | 00018000          | DDRA         | EOU             | \$18000              |         |        | LOCATION       | OF DATA I      | DIRECT       | ION REG        | SISTER A  |
| 11       00018000       DTRA       F00       +188004       LOCATTON OF CONTROL PACTSTER E         12       0000000       DTRA       F00       +FFFF       SETS ALL 16 A 11MES AS INPUTS         13       00002525       INITH       F00       +FFFF       SETS ALL 16 A 11MES AS INPUTS         14       00002525       INITH       F00       +12525       Will FTO       IDITTALIZE CRA         16       0000000       ACDRA       F00       +1400       +12525       Will FTO       IDITTALIZE CRA         16       0000000       ACDRA       F00       +1400       Will FTO       IDITTALIZE CRA         17       0000000       ACDRA       F00       +1400       Will FTO       IDITTALIZE CRA         18       00018002       MOVE 4       400F4+CRA       OFEN_DORA (16 BITS)         19       *       INTTTALIZE THE PIA'S       *         20       00018002       MOVE 4       400F4+CRA       OFEN_DORA (16 BITS)         20       00018002       MOVE 4       400F4+CRA       HAP0SHAKE PODE+INTERNOFT EMABLED         20       00018003       MOVE 4       400F4+CRA       F0FEN DORB (16 BITS)         20       00018004       MOVE 4       400F4+CRA       F0FEN DO                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 9      |            | 00018004          | DDRE         | EQU             | \$18004              |         |        | LOCATION       | OF DATA I      | DIRECT       | TON REC        | SISTER B  |
| 12       00000000       DTRA       FOU       40000       SETS ALL to A 1 MES AS IMPUTS         13       0000FFF       DTRA       FOU       4FFF       SETS ALL to A 1 MES AS UNPUTS         14       0000F525       TNTTA       FOU       4600       WHILE TO INITIAL TZE CRA         15       0000F0525       TNTTA       FOU       4600       WHILE TO INITIAL TZE CRA         16       0000000       ACDRA       FOU       46000       WHILE TO ACCESS DDRA THROUGH CRA         16       0000000       ACDRA       FOU       16000       WHILE TO ACCESS DDRA THROUGH CRA         17       0000000       ACDRA       FOU       16000       WHILE TO ACCESS DDRA THROUGH CRA         18       000000       SPECONO       NOTEA       FOU       16000       WHILE TO ACCESS DDRA THROUGH CRA         19       *       THTTALIZE THE PIA'S       THTTALIZE THE PIA'S       001600       1001800         20       00018000       NOVE-4       401RA-CDRA       A SUDE AS INPUT       NARCHERUPT ENABLED         20       00018000       NOVE-4       400RA-CRB       OFFN DDRA (16 ETS)       NOVE-4         20       00018000       NOVE-4       400RA-CRB       OFFN DDRA (16 ETS)       NOVE-4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1.0    |            | 00018002          | CRA          | EQU             | \$18002              |         |        | LOCATION       | OF CONTRO      | DL. RE.G     | ISTER (        | 9         |
| 13       0000FFF       0188       FOU       9FFFF       SETS ALL 16 E. LIMES AS OUTPUTS         14       00002325       INTTE       100       42525       WALLE TO BUTTALIZE DEA         16       0000000       ACDRS       FOU       9000       WALLE TO ACCESS DDRA THROUGH CRA         16       0000000       ACDRS       FOU       9000       WALLE TO ACCESS DDRA THROUGH CRA         18       *       INTTIALIZE THE PIA'S       *       INTIALIZE THE PIA'S         20       00018002       MOVE-4       #ACDFA-CRA       OPEN_DDRA (16 EITS)         20       00018002       MOVE-4       #ACDFA-CRA       OPEN_DDRA (16 EITS)         20       00018002       MOVE-4       #ACDFA-CRA       OPEN_DDRA (16 EITS)         20       00018002       MOVE-4       #ACDFA-CRA       OPEN DDRA (16 EITS)         20       0001800       MOVE-4       #ACDRB-CRB       OPEN DDRA (16 EITS)         20       00018006       MOVE-4       #ADDRB-CRB       E SIDE AS OUTPUT         20       00018006       MOVE-4       #ADDRB-CRB       DPEN DDRB (16 EITS)         20       00018006       MOVE-4       #ADDRB-CRB       E SIDE AS OUTPUT         20       00018006       MOVE-4       #                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1.1    |            | 00018006          | CRB          | EQU             | \$18005              |         |        | LOCATION       | OF CONTRO      | DL REG       | ISTER P        | 8         |
| 14       00002525       INITIA       EQU       4.2525       WALUE TO INITIALIZE DRA         15       00002035       INITIA       EQU       4.2525       WALUE TO INITIALIZE DRA         16       0000000       ACDRA       EQU       4.0000       WALUE TO ACCESS DDRA THROUCH TRA         18       *       INITIALIZE THE PIA'S       *       INITIALIZE THE PIA'S         20       *       INITIALIZE THE PIA'S       *         21       000000       33FC0000       MUVE.4       #ACDFA+CNA       OPEN_DDRA (16 BITS)         20       *       INITIALIZE THE PIA'S       *       *         20       *       INITIALIZE THE PIA'S       *         21       000000       33FC2525       MUVE.4       #ACDFA+CNA       OPEN_DDRA (16 BITS)         20       0001800       MUVE.4       #ACDRA+CNA       MANOSHAKE MODE + INTERRUPT ENABLED         24       0001800       MUVE.4       #ACDRB+CRB       DPEN DDRB (16 BITS)         20       0001800       MUVE.4       #ADDRB+CRB       DPEN DDRB (16 BITS)         26       00018004       MUVE.4       #ADDRB+DDRB       B SIDE AS OUTPUT         26       00018004       MUVE.4       #ADDRB+DDRB       B SIDE AS OUTPUT <td>1.2</td> <td></td> <td>00000000</td> <td>DIRA</td> <td>FOU</td> <td>\$0000</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 1.2    |            | 00000000          | DIRA         | FOU             | \$0000               |         |        |                |                |              |                |           |
| 15       00002525       TNTTE       F00       \$2525       VALUE TO IDITIOLIZE CRE         16       0000000       ACDRE       \$100000       VALUE TO ACCESS DDRE THROUGH CRE         17       0000000       SFC0000       *       *       INITIALIZE THE PIA*S         20       00018002       *       ACDE*+CRA       OPE*+0.DDRA (16 ETS)         20       00018002       #002.4       #ACDF*+CRA       OPE*+0.DDRA (16 ETS)         20       00018002       #002.4       #ACDR*+CRA       OPE*+0.DDRA (16 ETS)         20       00018004       #002.4       #ACDR*+CRB       OPE*+0.DDRA (16 ETS)         20       00018004       #002.4       #ACDR*+CRB       DFE*+0.DDRA (16 ETS)         20       00018004       #002.4       #ACDR*+CRB       DF*+0.DDRA (16 ETS)         21       00018004       #002.4       #ACDR*+CRB       DF*+0.DDR*+C         22       00018004       #002.4       #ADT*+CRB       #APOSHAKE P0DE+INTER/PT E                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 13     |            | 0000FFFF          | DIRE         | EQU             | \$FFFF               |         |        |                |                |              |                | 3         |
| 14       00000000       ACDRA       EOU       \$0000       Walde To ACCESS DDRA THROUGH CRA         19       *       DATTIALIZE THE PIA'S       Walde To ACCESS DDRA THROUGH CRA         20       *       DATTIALIZE THE PIA'S         21       000000       33FC0000       *         00018002       MOVE.4       #ACDFA+CRA       OPEN_DDRA (16 BITS)         20       00018002       MOVE.4       #DTRA+DDRA       A SIDE AS TAPUT         23       000010       33FC2525       MOVE.4       #DTRA+DDRA       A SIDE AS TAPUT         24       000018002       MOVE.4       #DTRA+DDRA       A SIDE AS TAPUT         24       000018003       MOVE.4       #DTRA+DDRA       A SIDE AS TAPUT         25       000018003       MOVE.4       #DTRA+DDRA       A SIDE AS TAPUT         24       000018004       MOVE.4       #ACDRB+CRB       DFEN DDRB (16 BITS)         25       000018004       MOVE.4       #ADTRB+DDRB       E SIDE AS UTFUT         26       010018004       MOVE.4       #ADTRB+DRB       E SIDE AS UTFUT         26       010018004       MOVE.4       #IDTRB+DRB       E SIDE AS UTFUT         27       *       *       *       *       *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |        |            | 00002525          | INITA        | EGU             | 42525                |         |        |                |                |              |                |           |
| 16       00010000       aCDRA       E00       \$0000       OACDE TO ACCESS DURK THROUGH CRA         17       0000000       aCDRA       FUO       \$0000       OACDE TO ACCESS DURK THROUGH CRA         18       *       IAUTIALIZE THE PIA'S       *         20       0001000       aCDESS DURK THROUGH CRA       *         21       001000       SBFC0000       *       *         00018002       mOVE.44       #ACDEA+CRA       DPEN_DDRA (16 BITS)         23       00018002       mOVE.44       #ACDEA+CRA       DPEN_DDRA (16 BITS)         24       00018002       mOVE.44       #ACDEA+CRA       HAMDSHAKE MODE + INTERRUPT ENABLED         24       00018004       mOVE.44       #ACDRB+CRB       DPEN DDRB (16 BITS)         25       000020       3BFC2255       mOVE.44       #ACDRB+CRB       DPEN DDRB (16 BITS)         26       0100200       BECFFFF       mOVE.44       #ACDRB+CRB       BISOC AS OUTPUT         26       010018004       mOVE.44       #ADDRB+CRB       BISOC AS OUTPUT         27       *       *       *       Figure 6. Initialization Routine         28       100018004       #ADDR       \$18005       \$18005         15       14 <td>15</td> <td></td> <td>00002525</td> <td>INITE</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 15     |            | 00002525          | INITE        |                 |                      |         |        |                |                |              |                |           |
| 19       *       INITIALIZE THE PIA'S         21       000000       33FC0000       00018002         20       00018002       00044       40784+0084       OPEN_DDRA (16 EITS)         20       00018002       0004600       MOVE.44       40784+0084       A SIDE AS TAPUT         20       00018006       MOVE.44       410174+084       HANOSHAKE MODE+INTERRUPT ENABLED         24       00018006       MOVE.44       410174+084       HANOSHAKE MODE+INTERRUPT ENABLED         24       00018006       MOVE.44       410174+084       HANOSHAKE MODE+INTERRUPT ENABLED         25       00018006       MOVE.44       410178+084       HANOSHAKE MODE+INTERRUPT ENABLED         26       00018006       MOVE.44       410178+084       HANOSHAKE MODE+INTERRUPT ENABLED         27       00018006       MOVE.44       410178+084       HANOSHAKE MODE+INTERRUPT ENABLED         28       *       *       Figure 6. Initialization Routine       Figure 6. Initialization Routine         18004       \$18005       \$18005       \$18005       Figure 6. Initialization Routine         1801       1802       0084       \$18005       Figure 6. Initialization Routine                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 1.6    |            | 00000000          | ACDRA        | EQU             |                      |         |        |                |                |              |                |           |
| 19       *       THETTALLZE THE PLA'S         20       00018002       00018002       00018002         00018002       00018002       00028.44       0028.40208         20       000100       33FC0000       00018002       00028.44         20       00018       33FC0000       00018002       00028.44         20       00018       33FC0000       00028.44       40084.420084       A SIDE AS INPUT         23       00018       33FC0000       00028.44       40084.420084       HAMOSHAKE MODE.INTERRUFT ENABLED         24       000018       33FC2555       00018004       MOVE.44       400784.0284       B SIDE AS OUTPUT         25       000018004       MOVE.44       400784.028       B SIDE AS OUTPUT         26       00018004       MOVE.44       400784.028       B SIDE AS OUTPUT         26       00018004       MOVE.44       10078.028       B SIDE AS OUTPUT         26       00018005       MOVE.44       10078.028       B SIDE AS OUTPUT         26       00018004       MOVE.44       110718.028       B SIDE AS OUTPUT         27       *       *       S18005       S18005         15       14       13       12       1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 17     |            | 00000000          | ACDEB        | EOU             | 4-0(00)1             |         |        | VALUE TO       | ACCESS D       | DEB TH       | ROUGH (        | SRE:      |
| 20       *         21       000000       33FC0000         00018002       MOVE.44       MACDFA+CRA       DPEN_DDRA (16 BITS)         22       000008       33FC0000       MOVE.44       MDRA+CDRA       A SLDE AS TNPUT         23       000100       33FC0000       MOVE.44       MDRA+CDRA       A SLDE AS TNPUT         23       000100       33FC0000       MOVE.44       MANDSHAKE MODE, INTERRUPT ENABLED         24       00018006       MOVE.44       MACDR8+CRB       DFEN_DDRB (16 BITS)         25       00018006       MOVE.44       MACDR8+CRB       DFEN_DDRB (16 BITS)         25       00018006       MOVE.44       MACDR8+CRB       DFEN_DDRB (16 BITS)         26       00018006       MOVE.44       MARDSHAKE MODE, INTERRUPT ENABLED         27       *       *       *       MANDSHAKE MODE, INTERRUPT ENABLED         28       *       *       *       *         Figure 6. Initialization Routine         \$18004         \$18005         *         \$18005         \$18005         *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |        |            |                   | *            |                 |                      |         |        |                |                |              |                |           |
| 21       00018002       33FC0000       00018002       00026.4       402644-CRA       0PEN_DDRA (16_ETTS)         22       000018000       00018000       00026.4       407RA+CDRA       A SIDE AS INPUT         23       000118002       00018002       00026.44       4107RA+CDRA       HANDSHAKE MODE+INTERRUPT ENABLED         24       00018003       00018004       00026.44       4107RA+CRA       HANDSHAKE MODE+INTERRUPT ENABLED         25       00018004       00018004       00026.44       4107RB+CRB       0PEN_DDRB (16_ETTS)         25       00018004       00018004       00026.44       4107TB+CRB       E_SIDE AS DUTFUT         26       00018004       00026.44       4107TB+CRB       HAMDSHAKE MODE+INTERPUPT ENABLED         27       00018004       00026.44       4107TB+CRB       HAMDSHAKE MODE+INTERPUPT ENABLED         27       *       *       Figure 6. Initialization Routine       Figure 5.         * Figure 6. Initialization Routine         \$18004         \$18005         * *         \$18005         \$18005         * *                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |        |            |                   | ж            | I.              | NITIALIZE THE        | e Pie.  | S      |                |                |              |                |           |
| 00018002       MOVE.4       #ACDFA+CRA       OPEN_DORA (16_BITS)         22       000008       33FC0000       MOVE.4       #DTRA+ODRA       A SIDE AS INPUT         23       000100       33FC2525       MOVE.4       #INITA+CRA       HANDSHAKE MODE+INTERRUPT ENABLED         24       00018000       MOVE.4       #ACDRB+CRB       OPEN_DORB (16_BITS)         24       00018004       MOVE.4       #ACDRB+CRB       OPEN_DORB (16_BITS)         25       000120       33FC6FFF       MOVE.4       #ACDRB+CRB       E_SIDE AS DUTPUT         26       00018004       MOVE.4       #INTTE+CRB       HAMOSHAKE MODE+INTERPUFT ENABLED         27       *       *       *       *       *         27       *       *       *       *       *         Figure 6. Initialization Routine         \$18004       \$18005         *         \$18004       \$18005         \$18004       \$18005         \$18004       \$18005         \$18004       \$18005         \$18004       \$18005         \$15       14       13       12       11       10 <t< td=""><td></td><td></td><td></td><td>ж</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |        |            |                   | ж            |                 |                      |         |        |                |                |              |                |           |
| 22       00000B       33FC0000<br>0001B000<br>33FC2525<br>0001013       MOVE.44       4DTRA+DDRA       A SIDE AS TAPUT         23       0001013       33FC2525<br>00018006       MOVE.44       4DTRA+DDRA       A SIDE AS TAPUT         24       00018006       MOVE.44       4DTRA+DDRA       HANDSHAKE MODE +INTERRUPT ENABLED         25       000020       33FC2525<br>00018006       MOVE.44       4DTRB+DDRB       E SIDE AS DUTFUT         26       00018006       MOVE.44       4DTRB+DDRB       E SIDE AS DUTFUT         27       *       MOVE.44       4DTRB+DDRB       E SIDE AS DUTFUT         28       *       MOVE.44       4DTRB+DRB       Ham0DSHAKE MODE +INTERPUPT ENABLED         27       *       *       *       Figure 6. Initialization Routine         *         \$18004       \$18005         \$18004       \$18005         \$18004       \$18005         \$18005       \$18005                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 21     | 000000     |                   |              |                 |                      |         |        |                |                |              |                |           |
| 0001000000000000000000000000000000000                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |        |            |                   |              | MOVELW          | #ACDFA .CRA          |         |        | OPEN DDR       | A (16 BITS     | 5)           |                |           |
| 23       000610       33FC2525<br>00018006       POVE.V       #INITA+CRA       HANDSHAKE MODE+INTERRUPT ENABLED         24       00018006       00018006       POVE.V       #ACDR8+CRE       OPEN DDR8 (16 EITS)         25       000120       33FC2525       POVE.V       #DTR8+DDRB       E SIDE AS DUTFUT         26       00018006       POVE.V       #DTR8+DDRB       E SIDE AS DUTFUT         26       00018006       POVE.V       #DTR8+DRB       HANDSHAKE PODE+INTERRUPT ENABLED         27       *       *       POVE.V       #DTR8+CRB       MANDSHAKE PODE+INTERRUPT ENABLED         27       *       *       Figure 6. Initialization Routine       Figure 5.         Figure 6. Initialization Routine         \$18004       \$18005         *         \$18004       \$18005                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 22     | 000008     |                   |              |                 |                      |         |        | to the Lorison | and a set of a |              |                |           |
| 00018002<br>24 000018 33FC2000<br>00018006<br>25 000020 33FCFFFF<br>00018004<br>26 000028 33FC2525<br>00018004<br>27 *<br>28 *       MOVE.4 #ACDR8+CR8<br>MOVE.4 #ACDR8+CR8<br>00FN DDR8 (16 EITS)         27<br>28       *<br>*         28       *         Figure 6. Initialization Routine                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 12.12  |            |                   |              | MOVELW          | #DIRA, DDRA          |         |        |                |                |              |                |           |
| 24       000016       33FC0000<br>00018006       MOVE · W #ACDRB · CRB       DPEN DDRB (16 ETTS)         25       000028       33FC2525       MOVE · W #DTRB · CRB       E SIDE AS OUTPUT         26       00018006       MOVE · W #DTRB · CRB       HervDSHAKE MODE · INTERRUPT ENABLED         27       *         28       *         Figure 6. Initialization Routine                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 23     | 000010     |                   |              |                 | amore cost           |         |        |                |                | DELE         | T PLACE        | Laterias. |
| 00018006       POVE.9       #ACDRB+CRE       OPEN DDR6 (16 EITS)         25 000020 33FCFFFF       POVE.9       #DDR5,DDRE       E SIDE AS DUTPUT         26 000028 33FC25225       POVE.9       #INTE+CRB       HAPDSHAKE PODE,INTERPUPT ENABLED         27       *         28       *         29       *         Figure 6. Initialization Routine         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18005         \$18004         \$18004         \$18005                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |                   |              | MUVE. W         | #INTIA*CRA           |         |        | HANDSHAR       | E MODE . TN    | HERROP.      | T ENABL        |           |
| 25       000020       33FCFFFF       0001B004       MOVE.V       #07RB,DDRB       B SIDE AS DUTFUT         26       000128       33FC2525       MOVE.V       #107RB,CDRB       HamDSHAKE MODE,INTERPUFT ENABLED         27       *         28       *       *         Figure 6. Initialization Routine         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18005         \$18004         \$18004         \$18005         \$18005         \$18004         \$18005         \$18005         \$18004         \$18005         \$15         \$14       13       12       11       10       9       8       7       6       5       4       3       2       1       0         \$15       14                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 2.4    | 000018     |                   |              | 54731 UP2 - 1.4 | A PERINE CERT        |         |        | onerst comp    | EN CAL FORM    |              |                |           |
| 00018004<br>26 000028 53FC2525<br>00018006       MOVE.W       DDRB       E SIDE AS DUTPUT         27<br>28       *       *       MANDSHAKE MODE, INTERPUET ENABLED         Figure 6. Initialization Routine         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18005         \$18004         \$18004         \$18005         \$18004         \$18005         \$18004         \$18005         \$18004         \$18005         \$18004         \$18005         \$18004         \$18005         \$18005         \$18004         \$18004         \$18005         \$18005         \$1800         \$180         \$180         \$180         \$180         \$2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 15421  | 000000     |                   |              | MUME + M        | WALLDICE & CITES     |         |        | OF EN DUR      | as the bulls   | 37           |                |           |
| 23       000128 33FC2525<br>000118005       PRIVE IIIVTIE + C.KB       HAMDSHAKE MODE + INTERPUPT ENABLED         27       *         28       *         Figure 6. Initialization Routine         \$18004         \$18004         \$18004         \$18005         15       14       13       12       11       10       9       8       7       6       5       4       3       2       1       0         1801       1802       CA2 Control       DDRA       CA1       1801       1802       CA2 Control       DDRA       CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 2      | 000020     |                   |              | SECTION 11      | 40300 BODD           |         |        | o eror a       | e oureur       |              |                |           |
| 100118003       MOUELULIPTIELCRB       HAMDSHAKE MODELINTERBUPT ENABLED         27       *         28       *         Figure 6. Initialization Routine         \$18004         \$18004         \$18004         \$18004         \$18004         \$18004         \$18005         \$18004         \$18004         \$18005         \$18004         \$18004         \$18005         \$18004         \$18005         \$18004         \$18004         \$18005         \$18004         \$18004         \$18005         \$18005         \$18004         \$18005         \$18004         \$18005         \$18005         \$1801       \$1802       \$242       \$2         \$1801       \$1802       \$242       \$2 <th< td=""><td>122</td><td>000000</td><td></td><td></td><td>NUME * M</td><td>HEULIND 7 LAURID</td><td></td><td></td><td>D DAUE P</td><td>is our or</td><td></td><td></td><td></td></th<>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 122    | 000000     |                   |              | NUME * M        | HEULIND 7 LAURID     |         |        | D DAUE P       | is our or      |              |                |           |
| 27     28     *       Figure 6. Initialization Routine       \$18004       \$18004     \$18005       15     14     13     12     11     10     9     8     7     6     5     4     3     2     1     0       Isolate     Isolate     Isolate     Isolate     Isolate     Isolate     Isolate       15     14     13     12     11     10     9     8     7     6     5     4     3     2     1     0       IB01     IB02     CA2 Control     DDRA     CA1     IB01     IB02     CA2 Control     DDRA     CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 2.0    | 000026     |                   |              | or 11 115 11    | A YALT DO . COD      |         |        | LAND CLIMP     | COMPANY - THE  | TELEVISIO DE | T CALMEN       | (ICT)     |
| Figure 6. Initialization Routine<br>\$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 17.7   |            | 00016008          | *            | 1:0.17515 # 24  | U 705 L LES & C. LES |         |        |                |                |              |                |           |
| Figure 6. Initialization Routine         \$18004       \$18005         15       14       13       12       11       10       9       8       7       6       5       4       3       2       1       0         IB01       IB02       CA2 Control       DDRA       CA1       IB01       IB02       CA2 Control       DDRA       CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |        |            |                   | .A.          |                 |                      |         |        |                |                |              |                |           |
| \$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 6.0    |            |                   | L. Alteração |                 |                      |         |        |                |                |              |                |           |
| \$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |            |                   |              | Fis             | gure 6. Initializa   | tion Ro | outine |                |                |              |                |           |
| \$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004 \$18005<br><u>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</u><br><u>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004 \$18005<br><u>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</u><br><u>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1</u>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004 \$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004<br>\$18005<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>UB01 UB02 CA2 Control DDRA CA1 UB01 UB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| \$18004<br>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0<br>IB01 IB02 CA2 Control DDRA CA1 IB01 IB02 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |        |            |                   | \$18004      |                 |                      |         |        |                | \$18005        |              |                |           |
| 15     14     13     12     11     10     9     8     7     6     5     4     3     2     1     0       IB01     IB02     CA2 Control     DDRA     CA1     IB01     IB02     CA2 Control     DDRA     CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
| IBO1 IBO2 CA2 Control DDRA CA1 IBO1 IBO2 CA2 Control DDRA CA1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |        |            |                   |              |                 |                      |         |        |                |                |              |                |           |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | -204 1 | 15         | 14 13 1           | 2 11         | 10              | 9 8                  | 7       | 6      | 5              | 4 3            | 2            | 00010          | 0         |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | dmiss  | 1111 16.01 | Consider Analisia | 11 12 50 310 | NOU00-11        | 1 2013. 1 11C IV     |         |        |                |                |              |                |           |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | quan   | IRQ1 I     | RQ2 CA2           | Control      |                 |                      | IRQ1    | IRQ2   | CAS            | 2 Control      | 10.250.062   | and the second | 2         |

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|------|------|-------------|----------------|----------------|------|------|-------------|----------------|----------------|
| IRQ1 | IRQ2 | CA2 Control | DDRA<br>Access | CA1<br>Control | IRQ1 | IRQ2 | CA2 Control | DDRA<br>Access | CA1<br>Control |

accessed. However, word operations on the MC68000 must CRA, U14 here here an another here

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# and searbles been feel and be been last i A of Figure 7. 16-Bit Control Register